CLAIMS

What is claimed is:

1. A flash memory cell comprising:

a substrate having a plurality of active regions; and

a floating gate structure disposed over the substrate, the floating gate structure extending across at least three of the active regions of the substrate;

wherein the floating gate structure and the at least three active regions define at least two channel regions dedicated for programming.

2. The flash memory cell according to claim 1, wherein the floating gate structure is associated with a source region of the substrate and further comprising a control gate structure at least partially disposed over the floating gate structure, the control gate structure associated with at least three drain regions of the substrate.

3. The flash memory cell according to claim 2, wherein the floating gate and control gate structures comprise a split gate structure.

4. The flash memory cell according to claim 2, further comprising an intergate dielectric disposed between the floating and control gate structures.

5. The flash memory cell according to claim 2, wherein the channel regions are disposed between the source region and each of the at least three drain regions.

6. A method of fabricating a flash memory cell, the method comprising the steps of:

providing a substrate having a plurality of active regions; and

forming a floating gate structure over the substrate and across at least three of the active regions of the substrate;

wherein the floating gate structure and the at least three active regions define at least two channel regions dedicated for programming.

7. The method according to claim 6, further comprising the step of forming a control gate structure at least partially over the floating gate structure.

8. The method according to claim 7, further comprising the steps of:

forming a source region in the substrate, the source region being associated with the floating gate structure; and

forming at least three drain regions in the substrate, the control gate structure being associated with the drain regions.

9. The method according to claim 7, wherein the floating gate and control gate structures comprise a split gate structure.

10. The method according to claim 7, further comprising the step of forming an intergate dielectric between the floating and control gate structures.

11. The method according to claim 8, wherein the channel regions are disposed between the source region and each of the at least three drain regions.

12. A method of programming a flash memory cell having a substrate including a plurality of active regions, a floating gate structure disposed over the substrate and associated with a source region of the substrate, the floating gate structure extending across at least three of the active regions of the substrate, the floating gate structure and the at least three active regions defining at least two channel regions dedicated for programming, and a control gate structure at least partially disposed over the floating gate structure, the control gate structure associated with at least three drain regions of the substrate, the method comprising the steps of:

applying a programming voltage to a first one of the at least three drain regions; and

applying an inhibiting voltage to a second one of the at least three drain regions.

13. The method according to claim 12, further comprising the step of applying an inhibiting voltage to a third one of the at least three drain regions.

14. A method of programming a flash memory cell having a substrate including a plurality of active regions, a floating gate structure disposed over the substrate and associated with a source region of the substrate, the floating gate structure extending across at least three of the active regions of the substrate, the floating gate structure and at least two of the at least three active regions defining two channel regions dedicated for programming, and a control gate structure at least partially disposed over the floating gate structure, the control gate structure associated with at least three drain regions of the substrate, the method comprising the steps of:

applying a programming voltage to a first one of the at least three drain regions; and

applying an inhibiting voltage to a second one of the at least three drain regions;

wherein the voltage applying steps are performed simultaneously.

15. The method according to claim 14, further comprising the step of applying an inhibiting voltage to a third one of the at least three drain regions.

16. The flash memory cell according to claim 1, wherein the memory cell comprises an EEPROM split-gate flash memory.

17. The method according to claim 6, wherein the memory cell comprises an EEPROM split-gate flash memory.

18. The method according to claim 12, wherein the memory cell comprises an EEPROM split-gate flash memory.

17. The method according to claim 14, wherein the memory cell comprises an EEPROM split-gate flash memory.